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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,676	07/04/2003	Chin-Long Lin	68146241-005011	7315

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EXAMINER	
STIGLIC, RYAN M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,676	LIN ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 and 13-18 are pending and have been examined.

2. Claims 1-11 and 13-18 are rejected.

Response to Arguments

3. Applicant's arguments, see Remarks pages 8 and 9, filed August 16, 2005, with respect to the rejection(s) of claim(s) 1, 6, and 11 under 35 U.S.C. § 102(b) and § 103(a) have been fully considered and are persuasive. The Examiner agrees with applicant that Huang et al. thus fails to teach a method and system in which the access priority grades are updated on a clock cycle basis, however upon further consideration Hewitt et al. teaches the limitation of updating the access priority grades on a clock cycle basis. Therefore the following prior art rejections are made in light of the amendments to the claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 4-8, 10-11, 13, and 15-18 rejected under 35 U.S.C. 102(b) as being anticipated by Hewitt et al. (US005956493A).

For claims 1 and 6 Hewitt discloses:

A system comprising: a plurality of functional devices accessing a memory (data) bus wherein said memory (data) bus allows access by one of said functional devices for one cycle of period of time;

- a plurality of request agents corresponding to said functional devices (Fig. 1, devices 122,140,170,172,174, and 176);
- a control register respectively storing access priority grades for said request agents (Fig. 2, 212; col. 4, ll. 45-53);
- a plurality of counter timers respectively loading said access priority grades (Fig. 2, 210; col. 4, ll. 30-44); and
- a bus elector coupled with said counter timers wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades (Fig. 2, 202; col. 4, line 54- col. 5, line 13);
- wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time (Figures 3A and 3B show two bus cycle where during the first bus cycle (Fig. 3A) REQ7 is granted access [referring to counter 7] and during a second bus cycle (Fig. 3B) REQ1 is granted access [referring to counter 1] and so on...); and
- wherein one or more of said access priority grades loaded in said counter timers are timely updated on a clock cycle basis (Hewitt teaches an arbitration method and system including programmable request latency counters that vary the priority of a requesting device according to the amount of time spent waiting to be granted access to a system

resource (col. 2, ll. 31-37; col. 4, line 11- col. 5, line 20). In particular, "As a lapse of time increases from when the peripheral device requested the bus, the level of arbitration priority for that peripheral increases." Since the level of arbitration priority is increase as a function of time, it (priority) is updated on a clock cycle basis (i.e. after X number of clock cycles the arbitration priority is increased)).

For claims 2 and 7 Hewitt discloses:

The system of claim 1 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces (Fig. 1, devices 122,140,170,172,174, and 176; col. 3, ll. 39-51).

For claims 3 and 8 Hewitt discloses:

The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value (col. 4, line 11- col. 5, line 20).

For claims 5 and 10 Huang teaches:

The system of claim 1 further comprising a control unit for connected to said request agents for respectively receiving corresponding requests for access to said memory bus (Fig. 1, "Bus Arbiter" 180; col. 3, line 61 – col. 5, line 49).

For claim 11 Hewitt teaches:

A method for a system having a plurality of functional devices accessing a memory bus, the method comprising the steps of:

- providing a plurality of request agents respectively corresponding to said functional devices (Fig. 1, devices 122,140,170,172,174, and 176);
- storing access priority grades for said request agents (Fig. 2, 212 & 210; col. 4, ll. 30-53);
- comparing said access priority grades (Fig. 2, 202; col. 4, line 54- col. 5, line 13);
- electing a request agent out of said request agents according to said compared access priority grades (Fig. 2, 202; col. 4, line 54- col. 5, line 13); and
- allowing access to said memory bus for one cycle of period of time by one of said functional devices corresponding to said elected request agent to said memory bus (Figures 3A and 3B show two bus cycle where during the first bus cycle (Fig. 3A) REQ7 is granted access [referring to counter 7] and during a second bus cycle (Fig. 3B) REQ1 is granted access [referring to counter 1] and so on...).
- wherein one or more of said access priority grades loaded in said counter timers are timely updated on a clock cycle basis (Hewitt teaches an arbitration method and system including programmable request latency counters that vary the priority of a requesting device according to the amount of time spent waiting to be granted access to a system resource (col. 2, ll. 31-37; col. 4, line 11- col. 5, line 20). In particular, "As a lapse of time increases from when the peripheral device requested the bus, the level of arbitration priority for that peripheral increases." Since the level of arbitration priority is increase as a function of time, it (priority) is updated on a clock cycle basis (i.e. after X number of clock cycles the arbitration priority is increased)).

For claim 13 Hewitt discloses:

The method of claim 11 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value (col. 4, line 11- col. 5, line 20).

For claim 15 Hewitt discloses:

The method of claim 11 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces (Fig. 1, devices 122,140,170,172,174, and 176; col. 3, ll. 39-51).

For claim 16-18 Hewitt discloses:

The method of claim 1(6 and 11) wherein updating said access priority grades stored in said counter timers includes decreasing one or more of said access priority grade values by a value of 1 (col. 4, line 30 – col. 5, line 49).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 9, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Hewitt in view of what was well known in the art at the time of applicant's invention.

For claims 4 and 9 Hewitt teaches:

The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value (The Examiner has previously shown that the invention of Hewitt selects competing requests on the basis of the smallest counter value representing a highest priority. Subtracting one from the current priority grade value of all denied sources dynamically alters the priority grade. OFFICIAL NOTICE is taken that it would have been obvious to one of ordinary skill in the pertinent art to add one to the initial priority grade values instead of subtracting one. The addition of one to all denied sources and the selection of the largest priority grade is functionally equivalent to subtracting one from all denied sources and selecting the competing source with the smallest priority grade. The Examiner respectfully submits that there is no significant novelty in implementing an addition/selecting largest priority scheme over a subtraction/selecting smallest priority scheme since the two schemes are functionally equivalent.).

8. Claims 1-11 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US006092137A) in view of Hewitt et al. (US005956493A) further in view of what was well known in the art at the time of applicant's invention.

For claims 1 and 6 Huang teaches:

A system comprising: a plurality of functional devices accessing a memory (data) bus wherein said memory (data) bus allows access by one of said functional devices for one cycle of period of time;

- a plurality of request agents corresponding to said functional devices (Fig. 2, CS#1 – CS#n);
- a control register respectively storing access priority grades for said request agents (While Huang does not expressly state the presence of said control register, they do teach an initial priority grade is assigned to each device (col. 5, ll. 22-24) during an initialization step performed by the arbiter (col. 6, ll. 1-2). Upon being granted use of the bus, a requesting device's priority grade is reset to its initial value (col. 5, ll. 30-33; col. 6, ll. 8-11). Furthermore if two competing sources share the same priority grade, the arbiter selects the competing source with the largest initial priority grade (col. 6, ll. 13-16). Therefore the arbiter [Fig. 2, 20] obviously contains some "control register" means for retrieving the initial priority grade of a device and comparing initial priority grades in the event of equivalent priority grades during arbitration.);
- a plurality of counter timers respectively loading said access priority grades (Fig. 2, 21-23; col. 4, ll. 59-67); and
- a bus elector coupled with said counter timers wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades (Fig. 2, 20; col. 5, line 63 – col. 6, line 16);

- wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time (Figure 3 shows that the process of requesting, arbitrating, and granting is repetitive [see the arrow leaving block S40]. Therefore the winning competing source is granted access to the bus for one cycle of period of time. Col. 5, ll. 28-30).

While Huang teaches updating the priority of a requesting device on the basis of time spent waiting to be granted they do not teach updating the priority grades in said counter timers on a clock cycle basis.

Hewitt teaches an arbitration method and system including programmable request latency counters that vary the priority of a requesting device according to the amount of time spent waiting to be granted access to a system resource (col. 2, ll. 31-37; col. 4, line 11- col. 5, line 20). In particular, "As a lapse of time increases from when the peripheral device requested the bus, the level of arbitration priority for that peripheral increases." Since the level of arbitration priority is increase as a function of time, it (priority) is updated on a clock cycle basis (i.e. after X number of clock cycles the arbitration priority is increased).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the request latency counters of Hewitt as the PMV counter/registers of Huang such that since the level of arbitration priority given to a peripheral device may be based

upon the length of time the peripheral has been waiting to gain ownership of the bus, improved overall system performance may be obtained, particularly for real time processing environments.

For claims 2 and 7 Huang teaches:

The system of claim 1 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces (The invention of Huang teaches implementing the invention with respect to peripheral interfaces (Media Access Controllers), col. 7, ll. 29-51; Fig. 8).

For claims 3 and 8 Huang teaches:

The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value (col. 5, ll. 20-36; Fig. 3 and 5; col. 5, line 63 – col. 6, line 16.).

For claims 4 and 9 Huang teaches:

The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value (The Examiner has previously shown that the invention of Huang selects a competing source on the basis of the smallest priority grade. Subtracting one from the current priority grade value of all denied sources dynamically alters the priority grade. OFFICIAL NOTICE is taken that it would have been obvious to one of ordinary skill in the pertinent art to add one to the initial priority grade values instead of subtracting one. The addition of one to all denied sources and

the selection of the largest priority grade is functionally equivalent to subtracting one from all denied sources and selecting the competing source with the smallest priority grade. The Examiner respectfully submits that there is no significant novelty in implementing an addition/selecting largest priority scheme over a subtraction/selecting smallest priority scheme since the two schemes are functionally equivalent.).

For claims 5 and 10 Huang teaches:

The system of claim 1 further comprising a control unit for connected to said request agents for respectively receiving corresponding requests for access to said memory bus (Fig. 1, "Arbiter" 6; all of Fig. 2; col. 5, line 63 – col. 6, line 16; col. 5, ll. 20-36).

For claim 11 Huang teaches:

A method for a system having a plurality of functional devices accessing a memory bus, the method comprising the steps of:

- providing a plurality of request agents respectively corresponding to said functional devices (Fig. 2, CS#1 – CS#n);
- storing access priority grades for said request agents (Fig. 2, 21-23; col. 4, ll. 59-67);
- comparing said access priority grades (Fig. 3, S36; col. 5, ll. 26-60);
- electing a request agent out of said request agents according to said compared access priority grades (col. 5, ll. 28-30); and
- allowing access to said memory bus for one cycle of period of time by one of said functional devices corresponding to said elected request agent to said memory bus

(Figure 3 shows that the process of requesting, arbitrating, and granting is repetitive [see the arrow leaving block S40]. Therefore the winning competing source is granted access to the bus for one cycle of period of time. Col. 5, ll. 28-30).

- wherein one or more of said access priority grades loaded in said counter timers are timely updated on a clock cycle basis (Hewitt teaches an arbitration method and system including programmable request latency counters that vary the priority of a requesting device according to the amount of time spent waiting to be granted access to a system resource (col. 2, ll. 31-37; col. 4, line 11- col. 5, line 20). In particular, "As a lapse of time increases from when the peripheral device requested the bus, the level of arbitration priority for that peripheral increases." Since the level of arbitration priority is increase as a function of time, it (priority) is updated on a clock cycle basis (i.e. after X number of clock cycles the arbitration priority is increased)).

For claim 12 Huang teaches:

The method of claim 11 further comprising the step of repeating steps (c), (d) and (e) for a plurality of cycles of period of time (Figure 3 shows that the process of requesting, arbitrating, and granting is repetitive [see the arrow leaving block S40]. Therefore the winning competing source is granted access to the bus for one cycle of period of time. Col. 5, ll. 28-30; col. 5, ll. 35-36).

For claim 13 Huang discloses:

The method of claim 11 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value (col. 5, ll. 20-36; Fig. 3 and 5; col. 5, line 63 – col. 6, line 16.).

For claim 14 Huang teaches:

The method of claim 11 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value (The Examiner has previously shown that the invention of Huang selects a competing source on the basis of the smallest priority grade. The priority grade is dynamically altered by subtracting one from the current priority grade value of all denied sources. OFFICIAL NOTICE is taken that it would have been obvious to one of ordinary skill in the pertinent art to add one to the initial priority grade values instead of subtracting one. The addition of one to all denied sources and the selection of the largest priority grade is functionally equivalent to subtracting one from all denied sources and selecting the competing source with the smallest priority grade. The Examiner respectfully submits that there is no significant novelty in implementing an addition/selecting largest priority scheme over a subtraction/selecting smallest priority scheme (since the two schemes are functionally equivalent.).

For claim 15 Huang teaches:

The method of claim 11 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral

interfaces (The invention of Huang teaches implementing the invention with respect to peripheral interfaces (Media Access Controllers), col. 7, ll. 29-51; Fig. 8).

For claim 16-18 Huang and Hewitt teach:

The method of claim 1(6 and 11) wherein updating said access priority grades stored in said counter timers includes decreasing one or more of said access priority grade values by a value of 1 (Huang; col. 5, ll. 20-37; Hewitt; col. 4, line 30 – col. 5, line 49).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS

PAUL R. MYERS
PRIMARY EXAMINER